TIMERS

General

COFFEE core has two independent built-in timers. Both timers are 32 bit wide and both have separate 8 bit divisor. Timers can be configured as watchdog timers or timer tick generators for system. Timer registers reside inside CCB (core configuration block) and can be accessed using ld and st instructions. Table 1 below explains the meaning and usage of timer registers.

Timer registers

Table 1, timer configuration and control registers

register mnemonic	bit field mnemonic	bits	explanation
TMR0_CNT		[31:0]	Current value of the timer0 counter. Can be set to arbitrary value.
TMR0_MAX_CNT		[31:0]	The maximum value of timer0 counter. Depending on CONT –bit, the timer will stop at maximum value or restart from zero. Note that, you can set a value greater than maximum count in TMR0_CNT –register in which case the timer counter will count to 0xffffffff and start over from zero.
TMR1_CNT		[31:0]	Current value of the timer1 counter. Can be set to arbitrary value.
TMR1_MAX_CNT		[31:0]	The maximum value of timer1 counter. Depending on CONT –bit, the timer will stop at maximum value or restart from zero. Note that, you can set a value greater than maximum count in TMR1_CNT –register in which case the timer counter will count to 0xffffffff and start over from zero.
TMR_CONF	TMR1_CONF	[31:16]	configuration bits for timer1. See table 2 for bit field definitions.
	TMR0_CONF	[15:0]	configuration bits for timer0. See table 2 for bit field definitions.

Table 2, Bit fields of configuration registers TMR1_CONF and TMR0_CONF

EN	31/15	EN = 1 enables timer. A timer can be stopped at any moment by writing EN = 0. Clearing EN bit will zero timer divider => timer will be incremented [DIV] + 1 clock cycles after enabling it.
CONT	30/14	CONT = 1: Continuous mode. Timer counter will start from zero after reaching maximum count defined in TMRx_MAX_CNT – register. CONT = 0: Timer counter will stop at maximum count.
GINT	29/13	GINT = 1: Generate an interrupt when maximum count is reached. GINT = 0: Do not generate interrupts.
WDOG	28/12	WDOG = 1: Enable watchdog function. If the timer reaches maximum count defined in TMRx_MAX_CNT the core will be reset.
-	27/11	Reserved, 0 or 1 can be written.
INTN	[26:24]/[10:8]	Bit field defining which interrupt to associate the timer with: “000” => EXT_INT0 ... “111” => EXT_INT7
DIV	[23:16]/ [7:0]	Divider value which defines how many clock cycles corresponds to one timer cycle: A timer counter will be incremented every [DIV] + 1 cycles, that is a zero value in DIV field sets the timer frequency to be the same as clock frequency of the core.

Notes:

- timer divider is usefull when clock frequency is reduced in order to save power. Only the DIV field has to be touched in order to maintain timing.