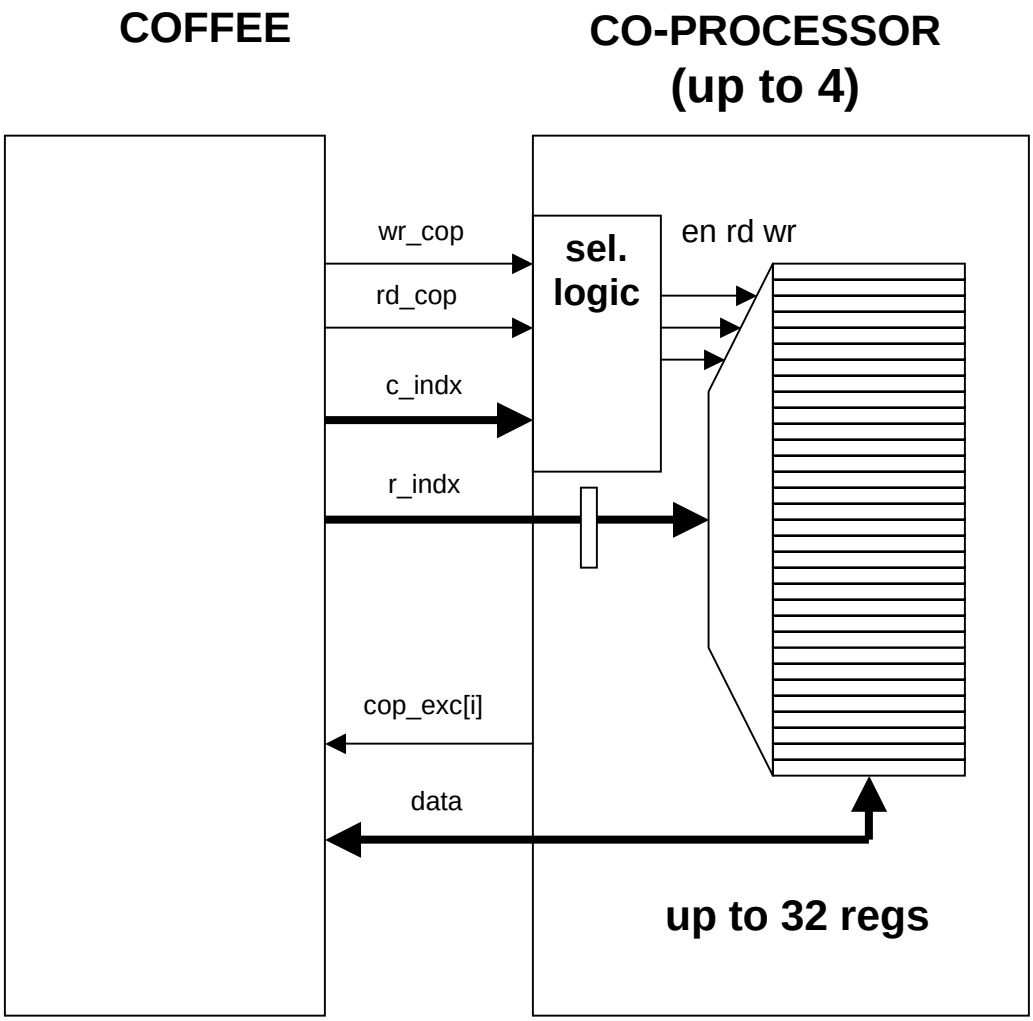
Interfacing coprocessors

Table 1, Coprocessor interfacing signals.

signal	Direction from the core side	purpose/description when active
COP_EXC[3..0]: COP_EXC(3) – COP 3 COP_EXC(2) – COP 2 COP_EXC(1) – COP 1 COP_EXC(0) – COP 0	In	Coprocessor exception. Coprocessor can interrupt the core by pulsing this signal.
COP_PORT(40): WR_COP	out	Write to cop. Write access to coprosessor register file.
COP_PORT(39): RD_COP	out	Read from cop. Read access to coprosessor register file.
COP_PORT[38..37]: C_INDX	out	Coprocessor index used to address one of the four possible coprocessors
COP_PORT[36..32]: R_INDX	out	Register index used to select the right register from the accessed coprocessor register bank.
COP_PORT[31..0]: DATA	inout	Data to/from the coprocessor.
stall	*in*	*Freezes the whole core! This signal does not strictly speaking belong to coprocessor interface but can be used if no other solution is available.*

[1] See document COFFEE_interface about signal type and timing specification.


COFFEE
CO-PROCESSOR
(up to 4)
wr_cop
rd_cop
c_indx
r_indx
sel.
logic
en rd wr
cop_exc[i]
data
up to 32 regs